

SANYO

No. 2576B

LB1644**Dual Bidirectional Motor Driver**

The LB1644 is a dual bidirectional motor driver. Since each channel has a 2-input logic circuit and performs bidirectional driving and braking functions, it is capable of direct driving 2pcs. of motor of various types rated at 6 to 24V. The output voltage can be varied by using external zener diodes. It is especially suited for dual motor drive (reel motor, loading motor, cassette motor in VTR) and for stepping motor drive.

Features

- . With power transistors for motor drive contained, capable of withstanding dash current of 1A max.
- . Performs braking function at the motor stop mode.
- . Contains elements to absorb motor dash current.
- . Input interfaceable to MOS LSI.
- . Minimum number of external parts required.
- . Wide operating voltage range.
- . Contains thermal shutdown protector.

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

			unit
Maximum Supply Voltage	$V_{CC\max}$	25	V
Input Voltage	V_{IN}	25	V
Output Current	I_{OUT}	± 1	A
Allowable Power Dissipation	$P_{d\max}$	1.44	W
Operating Temperature	T_{opr}	-25 to +65	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Allowable Operating Condition at $T_a=25^\circ\text{C}$

			unit
Supply Voltage	V_{CC}	7 to 25	V

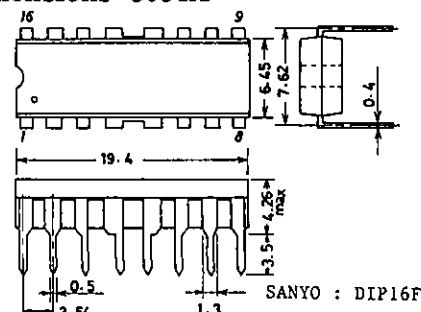
Electrical Characteristics at $T_a=25^\circ\text{C}$, $V_{CC}=12\text{V}$, per channel

			min	typ	max	unit
Current Dissipation	I_{CC1} Pin 1	Braking mode, $R_L=\infty$		8.0	11.5	mA
	I_{CC2} Pin 9	Braking mode, $R_L=\infty$		7.0	10.0	mA
Output Leakage Current	I_{OL}	Braking mode, $R_L=\infty$		40	120	μA
		per output pin				
Input Threshold Voltage	V_{th}	$R_L=\infty$	0.9	1.05	1.20	V
Output Voltage	V_o	$R_L=60\text{ohms}$, $V_Z=7.4\text{V}$	6.5	7.2	7.5	V

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Package Dimensions 3054A

(unit: mm)

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N3093TS/3251TS/6257KI, TS No.2576-1/5

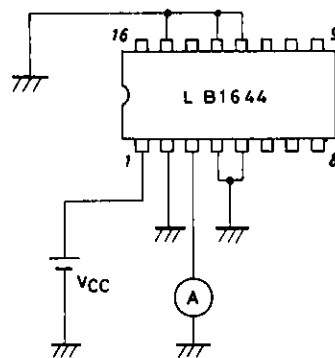
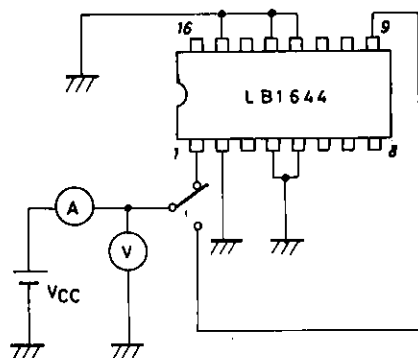
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		min	typ	max	unit
Output Tr Saturation	V_{sat1}		1.9	2.3	V
Voltage (Upper)			2.0	2.4	V
Output Tr Saturation	V_{sat2}		0.3	0.55	V
Voltage (Lower)			0.5	0.7	V

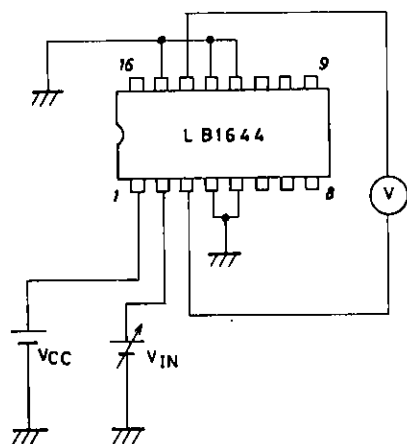
Test Circuits (per channel)(1) ICC1 (I_{pin})

ICC2 (9pin)

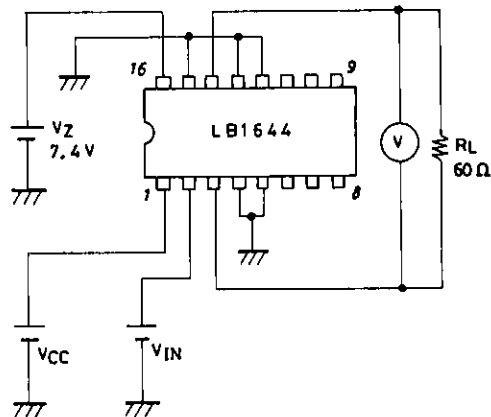
(2) IOL



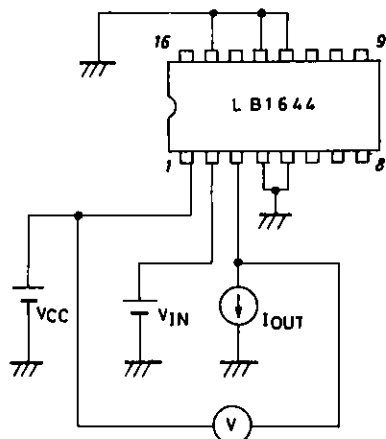
(3) Vth



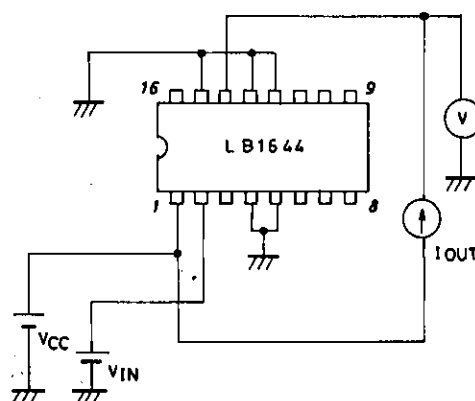
(4) Vo



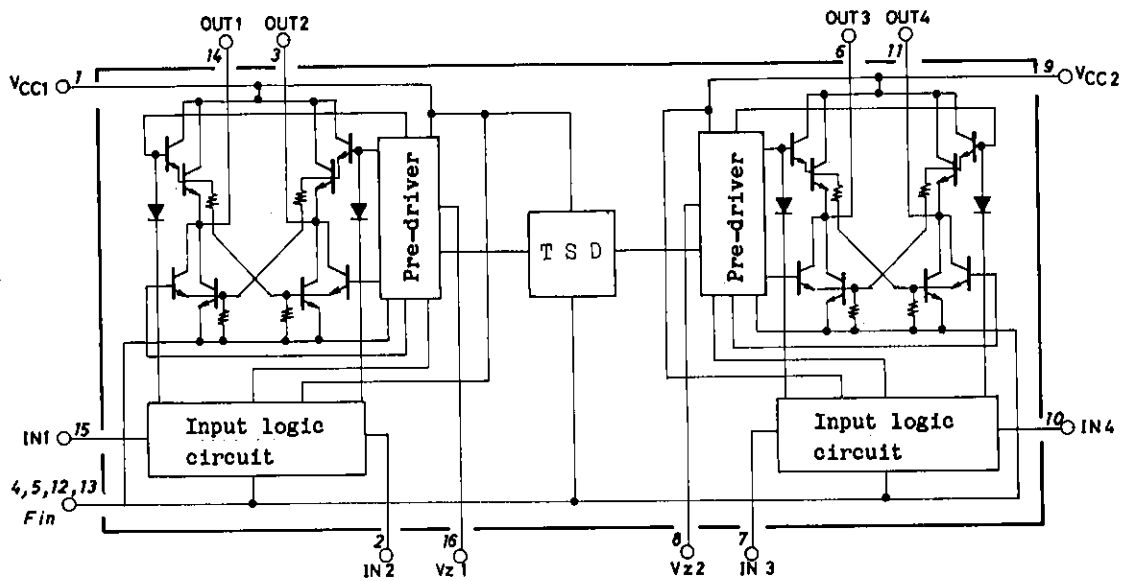
(5) Vsat1



(6) Vsat2



Equivalent Circuit Block Diagram



Truth Table of Logic Circuit

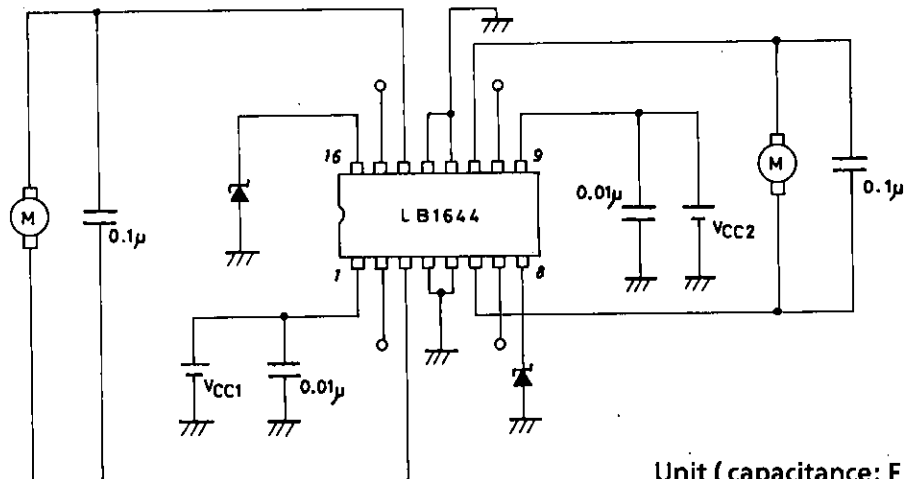
IN1	IN2	OUT1	OUT2	IN3	IN4	OUT3	OUT4
0	0	L	L	0	0	L	L
1	0	H	L	1	0	H	L
0	1	L	H	0	1	L	H
1	1	L	L	1	1	L	L

(Note) A capacitor of 0.01 μ F or greater must be connected across $V_{CC1,2}$ and GND.

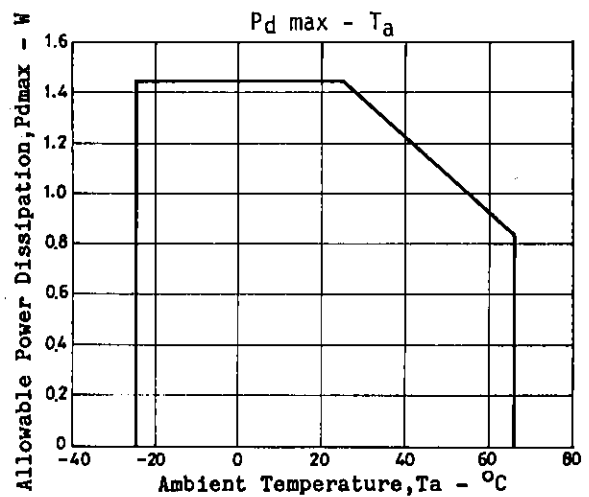
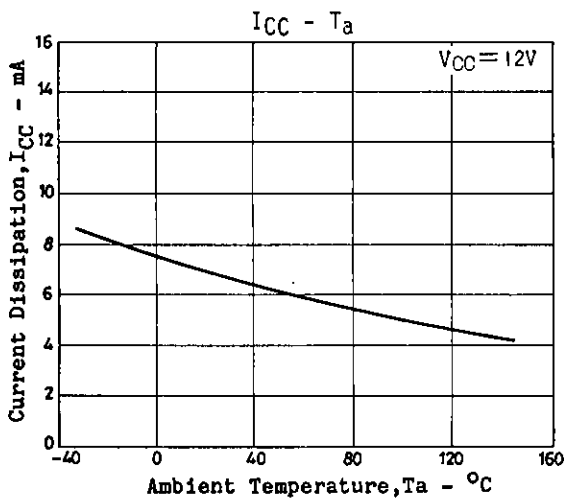
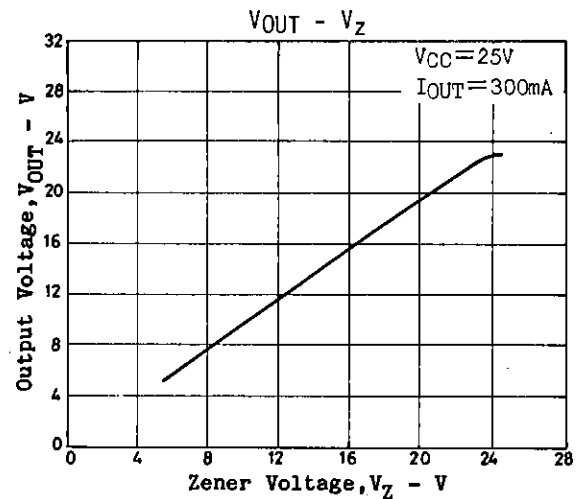
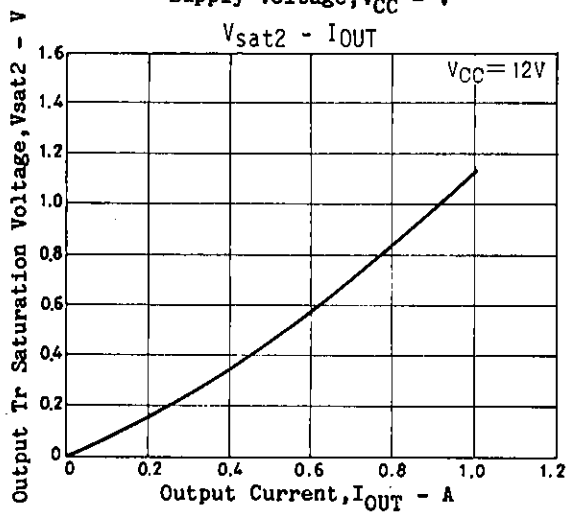
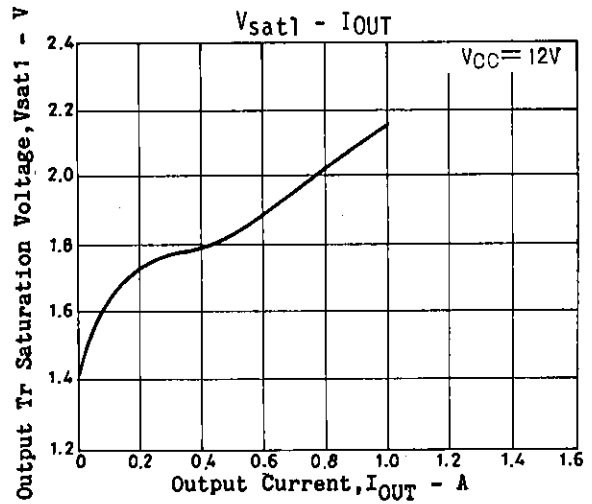
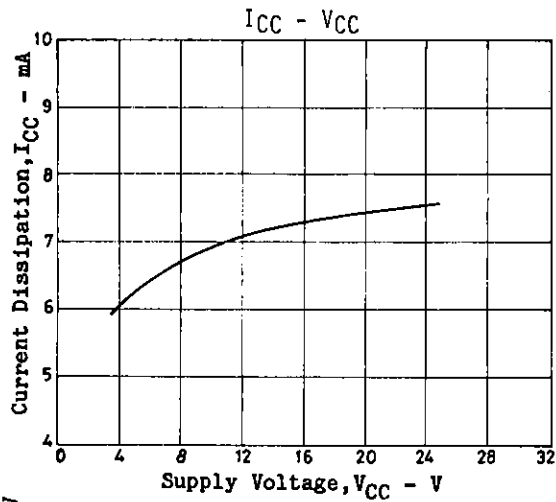
INPUT			OUTPUT				MODE	
IN1	IN2,3	IN4	OUT1	OUT2	OUT3	OUT4	M1	M2
0	0	0	L	L	L	L	Braking	Braking
1	0	0	H	L	L	L	Forward/reverse	Braking
0	1	1	L	H	L	L	Reverse/forward	Braking
1	1	0	L	L	H	L	Braking	Forward/reverse
0	0	1	L	L	L	H	Braking	Reverse/forward
1	1	1	L	L	L	L	Braking	Braking

The remaining input states 1,0,1 and 0,1,0 are not inhibited.

Sample Application Circuit



Unit (capacitance: F)



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